PATENT
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Application of:	)	
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Hee Youl LEE	)	
	)	Group Art Unit: Unknown
Application No.: To be assigned	)	
	)	
	)	Examiner: Unknown
Filed: Concurrently herewith	)	
	)	
For: METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE	)	

Commissioner for Patents
Washington, D.C. 20231

Sir:

PRELIMINARY AMENDMENT

Prior to the examination of the above-identified application, please amend the above-identified application as follows:

IN THE CLAIMS:

Please replace claims 1-10, with the following:

1.(Amended) A method of manufacturing a semiconductor device, comprising the steps of:

forming a patterned tunnel oxide film, a floating gate electrode, a dielectric film, and a control gate electrode in a cell region of a semiconductor substrate;

forming a gate electrode in a peripheral circuit region of the semiconductor substrate;

removing an exposed portion of a device isolation film in the cell region by a self-align source etch process;

forming a first capping layer and a second capping layer on the semiconductor substrate;

performing a self-align source annealing process for the cell region;

forming a source and drain junction in the cell region;

forming a low concentration source and drain junction in the peripheral circuit region; forming a gate spacer in the peripheral circuit region; and

forming a high concentration source and drain junction in the peripheral circuit region.

2.(Amended) The method according to claim 1, wherein a thickness of the first capping layer is 100-200Å.

3.(Amended) The method according to claim 1, wherein a thickness of the second capping layer is 50-150Å.

4.(Amended) The method according to claim 1, wherein the gate spacer is formed of the first capping layer, the second capping layer, and an oxide film by a blanket etch process.

5.(Amended) The method according to claim 4, wherein a thickness of the oxide film is 1200-1600Å.

6.(Amended) The method according to claim 4, wherein the oxide film and the first capping layer are etched through to lateral portions of the second capping layer to form a screen oxide film.

7.(Amended) The method according to claim 1, wherein the source and drain junction in the cell region is formed by using the first capping layer and the second capping layer as an ion implantation screen oxide film.

8.(Amended) The method according to claim 1, wherein the low concentration source and drain junction in the peripheral circuit region is formed by using the first capping layer and the second capping layer as an ion implantation screen oxide film.

9.(Amended) The method according to claim 1, wherein the high concentration source and drain junction in the peripheral circuit region is formed by using a lateral portion of the first capping layer etched as an ion implantation screen oxide film.

10.(Amended) The method according to claim 1, wherein the first capping and the second capping layer prohibit formation of a local bird's beak of the dielectric film formed between the floating gate electrode and the control gate electrode.

Conclusion

The foregoing amendments are being made to place the application in condition for examination. A favorable action on the merits is respectfully solicited.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attachment is captioned "Version with markings to show changes made."

If there are any other fees due in connection with the filing of this paper, please charge the fees to our Deposit Account No. 50-0310. If a fee is required for an extension of time under 37 C.F.R. § 1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account.

Respectfully Submitted,

By: ______________________
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Dated: December 7, 2001

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Claim 1 has been amended as follows:

1.(Amended) A method of manufacturing a semiconductor device, comprising the steps of:

~~[providing a semiconductor substrate in which a cell region and a peripheral circuit region are defined;]~~

forming a patterned tunnel oxide film, a floating gate electrode**, a dielectric film,** and a control gate electrode in ~~[said]~~ **a** cell region ~~[forming a gate electrode in said peripheral circuit region]~~ **of a semiconductor substrate;**

forming a gate electrode in ~~[said]~~ **a** peripheral circuit region **of the semiconductor substrate**;

removing an exposed portion of a device isolation film in ~~[said]~~ **the** cell region by ~~[means of]~~ a ~~[self-align]~~ **self-align** source etch process;

forming a first capping layer and a second capping layer on the ~~[entire structure]~~ **semiconductor substrate**;

performing a ~~[self-align]~~ **self-align** source annealing process for ~~[said]~~ **the** cell region;

forming a source and drain junction in ~~[said]~~ **the** cell region ~~[and]~~**;**

forming a low concentration source and drain junction in ~~[said]~~ **the** peripheral circuit region;

forming a gate spacer in ~~[said]~~ **the** peripheral circuit region; and

forming a high concentration source and drain junction in ~~[said]~~ **the** peripheral circuit region.

Claim 2 has been amended as follows:

2.(Amended) The method ~~[of manufacturing a semiconductor device]~~ according to claim 1, wherein ~~[said first capping layer is formed in thickness of 100 ~ 200 Å]~~ **a thickness of the first capping layer is 100-200Å**.

Claim 3 has been amended as follows:

3.(Amended) The method ~~[of manufacturing a semiconductor device]~~ according to claim 1, wherein ~~[said second capping layer is formed in thickness of 50 ~ 150 Å]~~ **a thickness of the second capping layer is 50-150Å**.

Claim 4 has been amended as follows:

4.(Amended) The method ~~[of manufacturing a semiconductor device]~~ according to claim 1, wherein ~~[said]~~ **the** gate spacer is formed of ~~[said]~~ **the** first capping layer~~[/]~~, ~~[said]~~ **the** second capping layer~~[/]~~, **and** an oxide film ~~[for a spacer in a way that an oxide film for a spacer is formed on said second capping layer and said oxide film for a spacer and said second capping layer are then sequentially etched]~~ by a blanket etch process.

Claim 5 has been amended as follows:

5.(Amended) The method ~~[of manufacturing a semiconductor device]~~ according to claim 4, wherein ~~[said oxide film for a spacer is formed in thickness of 1200 ~ 1600 Å]~~ **a thickness of the oxide film is 1200-1600Å**.

Claim 6 has been amended as follows:

6.(Amended) The method ~~[of manufacturing a semiconductor device]~~ according to claim 4, wherein ~~[said]~~ **the** oxide film ~~[for a spacer]~~ and ~~[said]~~ **the** first capping layer are etched through ~~[the mediation]~~ **to lateral portions** of ~~[said]~~ **the** second capping layer to form a screen oxide film.

Claim 7 has been amended as follows:

7.(Amended) The method ~~[of manufacturing a semiconductor device]~~ according to claim 1, wherein ~~[said]~~ **the** source and drain junction in ~~[said]~~ **the** cell region is formed by using ~~[said]~~ **the** first capping layer and ~~[said]~~ **the** second capping layer as an ion implantation screen oxide film.

Claim 8 has been amended as follows:

8.(Amended) The method ~~[of manufacturing a semiconductor device]~~ according to claim 1, wherein ~~[said]~~ **the** low concentration source and drain junction in ~~[said]~~ **the** peripheral circuit region is formed by using ~~[said]~~ **the** first capping layer and ~~[said]~~ **the** second capping layer as an ion implantation screen oxide film.

Claim 9 has been amended as follows:

9.(Amended) The method ~~[of manufacturing a semiconductor device]~~ according to claim 1, wherein ~~[said]~~ **the** high concentration source and drain junction in ~~[said]~~ **the** peripheral circuit region is formed by using **a lateral portion of** ~~[said]~~ **the** first capping layer etched ~~[by a given thickness]~~ as an ion implantation screen oxide film.

Claim 10 has been amended as follows:

10.(Amended) The method ~~[of manufacturing a semiconductor device]~~ according to claim 1, wherein ~~[said]~~ **the** first capping and ~~[said]~~ **the** second capping layer ~~[functions to]~~ prohibit **formation of** a local bird's beak of ~~[said]~~ **the** dielectric film formed between ~~[said]~~ **the** floating gate electrode and ~~[said]~~ **the** control gate electrode.